19-0085; Rev 0; 3/05

MAX3975 Evaluation Kit

Evaluates: MAX3975

General Description

The MAX3975 evaluation kit (EV kit) is an assembled demonstration board that provides complete optical and electrical evaluation of the MAX3975 VCSEL driver.

The EV kit is composed of two independent sections, one optical and one electrical, with a score line between the sections for optional separation. The output of the electrical section has a SMA connector that can be connected to a 50Ω terminated oscilloscope. The output of the optical section is configured for attachment to a VCSEL TOSA flex cable.

The optical section includes the DS1862* controller IC for testing closed-loop power control.

*Future Product

Features

- **Fully Assembled and Tested**
- **Allows Optical and Electrical Evaluation**
- **Easy Programming of Bias and Modulation Currents**
- **AC-Coupling Provided On-Board**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX3975EVKIT	0°C to +85°C	20 UCSP-20

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C4, C5, C9	4	0.1μF ±10% ceramic capacitors (0201)
C2, C3, C13, C16, C18, C20, C24, C25, C26	9	0.1μF ±5% ceramic capacitors (0402)
C6, C14, C23	3	10μF ±5% tantalum capacitors (B case)
C7, C10, C12, C15	4	1000pF ±5% ceramic capacitors (0201)
C8, C11, C17, C21	4	0.01μF ±5% ceramic capacitors (0402)
C19	1	Open
C22	1	1000pF ±5% ceramic capacitor
J1–J5	5	SMA connectors (edge mount, tab contact) EF Johnson 142-0701-851
J7, J10, J11, J18, J19, TP1–TP24	29	Test points Digi-Key 5000K-ND
JU1, JU3, JU4, JU7–JU11, JU13, JU16	10	2-pin headers, 0.1in centers Digi-Key S1012-36-ND
JU2, JU5, JU6, JU12, JU14, JU15	6	3-pin headers, 0.1in centers Digi-Key S1023-36-ND
JU1–JU16	16	Shunts Digi-Key S9000-ND
L1, L3, L6	3	1μH ±5% chip inductors Panasonic ELJFD1R0KF
L2, L4, L7	3	Ferrite beads (0603) Murata BLM18HK331SN1
L5**	1	VCSEL TOSA with 50Ω flex Advanced Optical Components HFE6190-561
Q1, Q2	2	P-Channel MOSFETs Fairchild FDN302P
R1, R7	2	1kΩ ±1% resistor (0402)
R2, R4, R5, R16	4	825Ω ±1% resistors (0402)
R3, R6, R10, R11	4	20kΩ variable resistors
R8	1	511kΩ ±1% resistor (0402)
R9	1	7.5kΩ ±1% resistor (0402)
R12	1	26.7kΩ ±1% resistor (0402)
R13	1	20.0kΩ ±1% resistor (0402)
R14, R15, R17, R18, R19	5	4.7kΩ ±5% resistor (0402)
R20	1	499Ω ±1% resistor (0402)
U1, U2	2	MAX3975UBA (20 UCSP-20)
U5	1	MAX9039BEBT (6 UCSP-6)
U6*	1	DS1862 25-ball STPBGA
None	1	MAX3975 EV kit circuit board, Rev A

*Future Product

**Component not included with EV kit

Component Suppliers

SUPPLIER	PHONE	FAX
Advanced Optical Components	866-698-2735	972-470-4654
AVX	843-448-9411	843-626-3123
Digi-Key	800-344-4539	218-681-3380
Murata	770-436-1300	770-436-3030
Panasonic	201-392-4818	201-392-6263

Note: *Please indicate that you are using the MAX3975 when ordering from these suppliers.*

Electrical Quick Start

The electrical section of the evaluation board requires a positive and negative supply in order for the output termination to electrically emulate the characteristics of a VCSEL. For more information, refer to Figure 1 in the MAX3975 datasheet. If desired, the electrical section of the board can be separated from the optical section by bending the board length-wise until they snap apart. Follow the procedure below to configure the electrical section for evaluation.

1) Place a shunt on JU3. This connects the BIASSET pin to the $R_{BIASSET}$ variable resistor (R11).
2) Place a shunt on JU4. This connects the MODSET pin to the R_{MODSET} variable resistor (R10).
3) Place a shunt on JU1. This enables the driver output by connecting the DISABLE pin to V_{EE}.
4) Adjust R11 until there is 2.4kΩ resistance between TP5 and TP6. This sets the output bias current to approximately 5mA.
5) Adjust R10 until there is 2.4kΩ resistance between TP4 and TP6. This sets the output modulation current to approximately 5mA.
6) Apply a 10Gbps differential signal (650mVp-p) between SMA connectors J1 (IN+) and J2 (IN-).
7) Connect an oscilloscope with a 50Ω termination to SMA connector J3 (OUT). The output must be DC-coupled to the oscilloscope.
8) Connect a +1.2V supply to J7 (V_{CC}), a –2.1V supply to J11 (V_{EE}), and the supply ground to J10 (GND).
9) Verify there is +1.2V at the V_{CC} pin by measuring the voltage from TP8 to TP7 and adjusting the voltage at J7 accordingly.
10) Verify there is –2.1V at the V_{EE} pin by measuring the voltage from TP6 to TP7 and adjusting the voltage at J11 accordingly.
11) Test the driver output current monitor by measuring the voltage from TP3 to TP6.
12) Adjust the variable resistor R11 until the desired bias current is achieved.
13) Adjust the variable resistor R10 until the desired modulation current is achieved.

Optical Quick Start

The optical section of the evaluation board requires installation of the VCSEL TOSA with flex cable (not included with EV Kit). The flex cable should be soldered to the board so that the TOSA points toward the top of the board. If desired, the optical section of the board can be separated from the electrical section by bending the board length-wise until they snap apart. Follow the procedure below to configure the optical section for evaluation.

1) Place shunts on JU6, JU7, JU8, JU9, JU10, JU11, JU13, and JU16.
2) Place a shunt across pins 1 and 2 of JU2. This connects the BIASSET pin to the $R_{BIASSET}$ variable resistor (R6).
3) Place a shunt across pins 1 and 2 of JU5. This connects the MODSET pin to the R_{MODSET} variable resistor (R3).
4) Move the shunt on JU6 to the side labelled GND.
5) Place shunts across pins 1 and 2 of JU12, JU14, and JU15.
6) Adjust R6 until there is 6kΩ resistance between TP2 and ground. This sets the output bias current to approximately 2mA.
7) Adjust R3 until there is 6kΩ resistance between TP1 and ground. This sets the output modulation current to approximately 2mA.
8) Apply a 10Gbps differential signal (650mVp-p) between SMA connectors J4 (IN+) and J5 (IN-).
9) Use a multi-mode fiber to connect the VCSEL TOSA to an optical-to-electrical converter or optical power meter.
10) Connect a +3.3V supply to J19 (V_{CC1}) and the supply ground to J18 (GND). The power-on-reset circuit will apply power to the VCSEL and V_{CC2} when V_{CC1} reaches approximately 2.9V.
11) Verify there is +3.3V at the V_{CC} pin by measuring the voltage from TP22 to ground and adjusting the voltage at J19 accordingly.
12) Adjust the bias current with R6 and the modulation current with R3 until the desired optical average power and amplitude is achieved.
13) Test the driver output current monitor by measuring the voltage from TP9 to ground.

Evaluation with closed loop power control requires the DS1862 controller (U6). Contact Dallas Semiconductor

technical support (pots.support@dalsemi.com) for the software and hardware required to program and communicate with the DS1862. The following steps will configure the optical section for using the DS1862.

14) Move the shunt on JU6 to the side labelled FETG. This connects the safety fault output of the controller to the MOSFET gate.

15) Move the shunt on JU2 to pins 2 and 3. This connects the BIASSET pin to the controller BIAS_DR pin.

16) Move the shunt on JU5 to pins 2 and 3. This connects the MODSET pin to the controller MOD_DR pin.

17) Using the DS1862 software, program the controller to achieve the desired average optical power and modulation amplitude.

18) The VCSEL monitor diode current can be determined by removing the shunt from JU10 and measuring the voltage across the two pins. The monitor diode current is equal to the measured voltage divided by 499Ω.

Adjustment and Control Descriptions (see Quick Start first)

COMPONENT		NAME	FUNCTION
OPTICAL	ELECTRICAL		
JU7	JU1	DISABLE	Enables/disables the driver output currents. Place a shunt on JU1 or JU7 to enable the output currents.
–	JU3	–	Connects the BIASSET pin to the $R_{BIASSET}$ variable resistor (R11).
–	JU4	–	Connects the MODSET pin to the R_{MODSET} variable resistor (R10).
JU2	–	–	Connects the BIASSET pin to either the $R_{BIASSET}$ variable resistor (R6) or to the BIAS_DR pin of the DS1862. Shunt pins 1 and 2 to use the $R_{BIASSET}$ resistor. Shunt pins 2 and 3 to use the DS1862.
JU5	–	–	Connects the MODSET pin to either the R_{MODSET} variable resistor (R3) or the MOD_DR pin of the DS1862. Shunt pins 1 and 2 to use the R_{MODSET} resistor. Shunt pins 2 and 3 to use the DS1862.
R6	R11	$R_{BIASSET}$	Adjusts the driver bias current. Rotate clockwise to increase the bias current.
R3	R10	R_{MODSET}	Adjusts the driver modulation current. Rotate clockwise to increase the modulation current.
JU6	–	–	Connects the MOSFET gate to either ground or the FETG pin of the DS1862.
JU8	–	V_{CC2}	Connects the V_{CC1} power plane to the V_{CC2} power plane.
JU9	–	AUX1	Connects the MONITOR pin to the AUX1 pin of the DS1862.
JU10	–	MD	Connects the VCSEL monitor diode to the I_{MD} pin of the DS1862. The VCSEL monitor diode current can be determined by removing the shunt from JU10 and measuring the voltage across the two pins. The monitor diode current is equal to the measured voltage divided by 499Ω.
JU11	–	MOD_DESEL	Enables/disables the communication with the DS1862 over the 2-wire interface bus (SDA and SCL). Place a shunt on JU11 to enable communication on the bus.

Adjustment and Control Descriptions (continued)

COMPONENT		NAME	FUNCTION
OPTICAL	ELECTRICAL		
JU12	–	SC_TX_LOL	Sets the SC_TX_LOL pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU13	–	P_DOWN	Enable/disables the power down mode of the DS1862. Remove the shunt to enable power down mode.
JU14	–	SC_RX_LOS	Sets the SC_RX_LOS pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU15	–	SC_RX_LOL	Sets the SC_RX_LOL pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU16	–	TX_DIS	Control pin of the DS1862 used to enable/disable the bias and modulation currents. Place a shunt on JU16 to enable the currents.

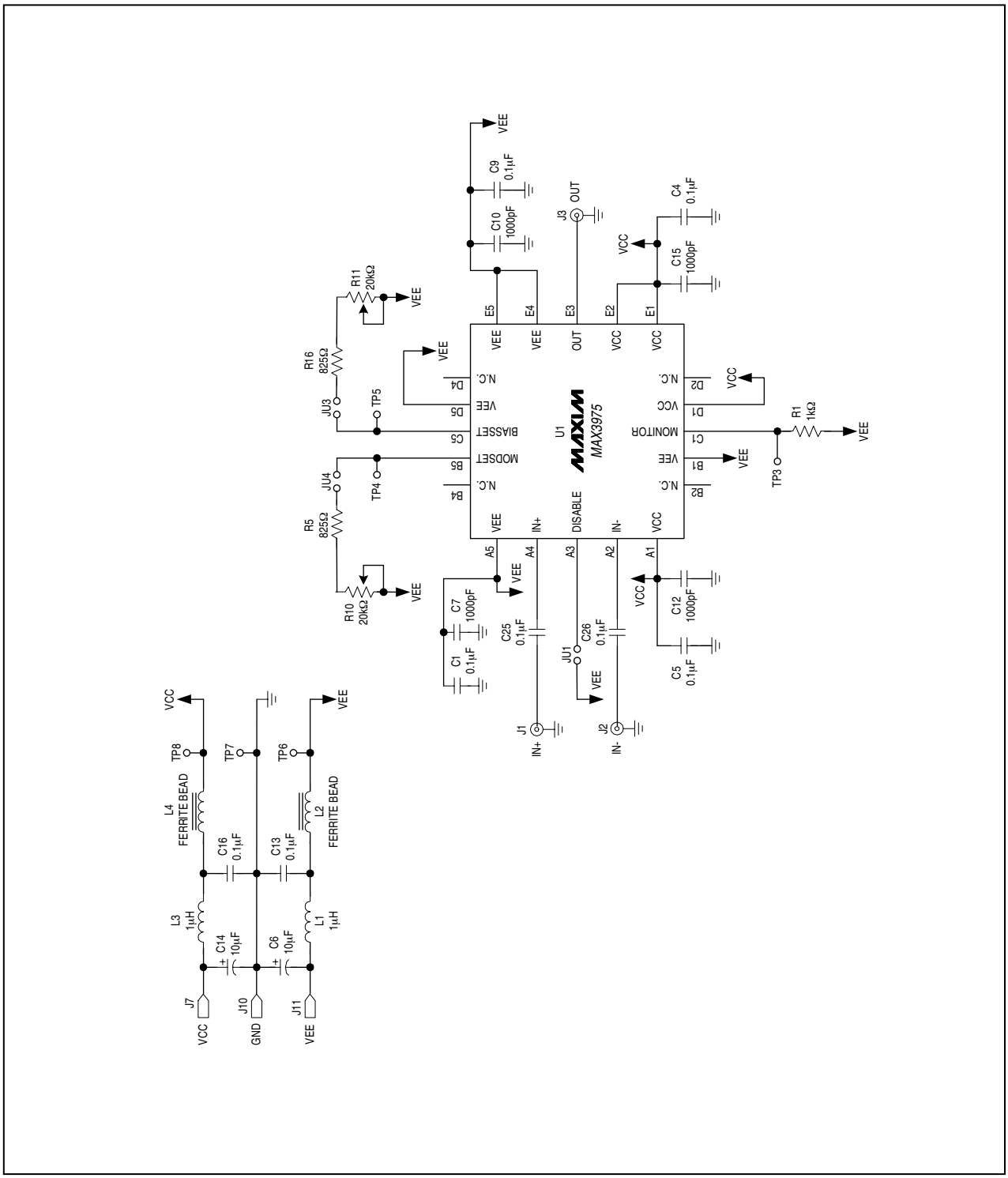

Figure 1. MAX3975 EV Kit Schematic – Electrical Section

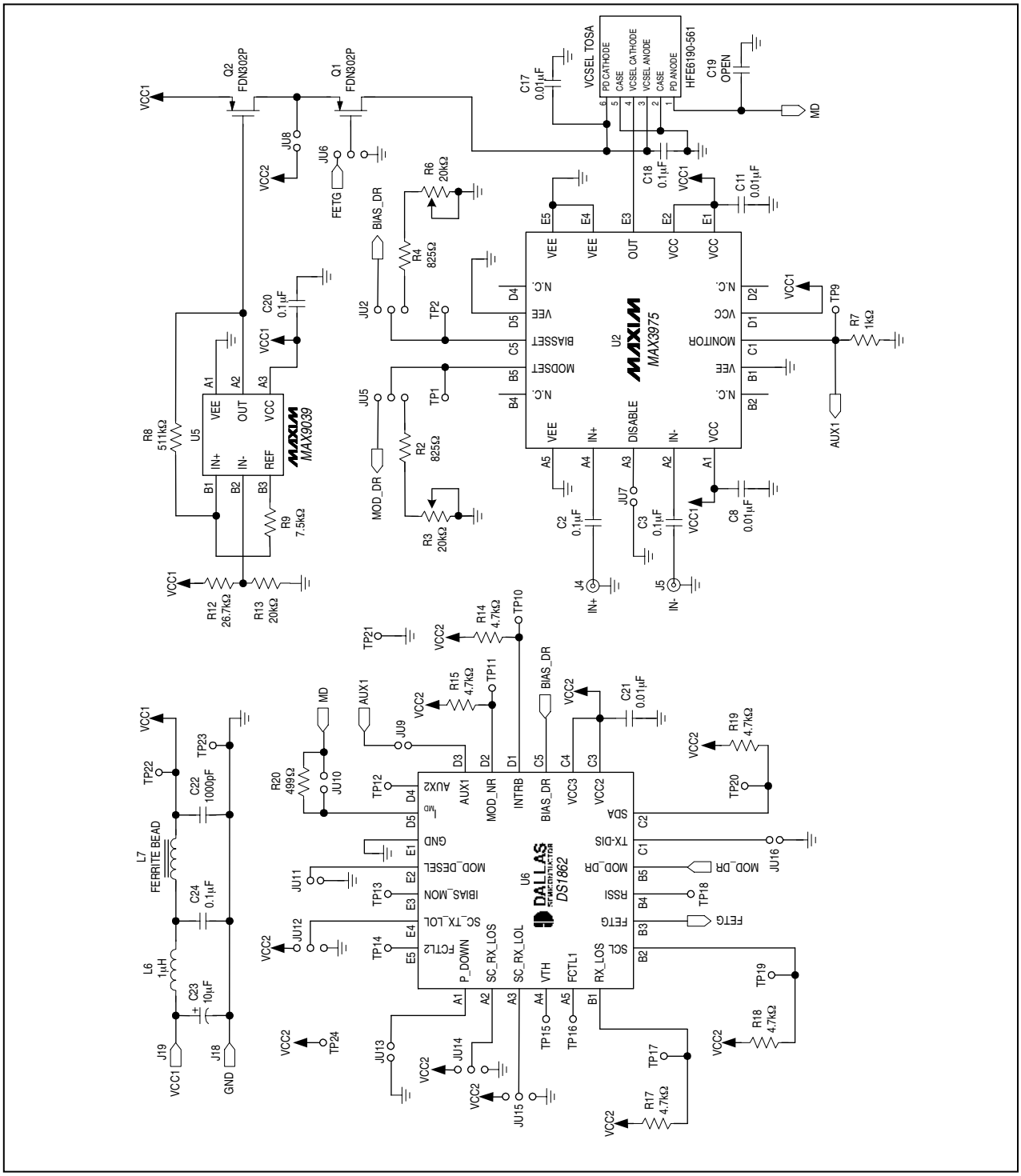

Figure 2. MAX3975 EV Kit Schematic – Optical Section

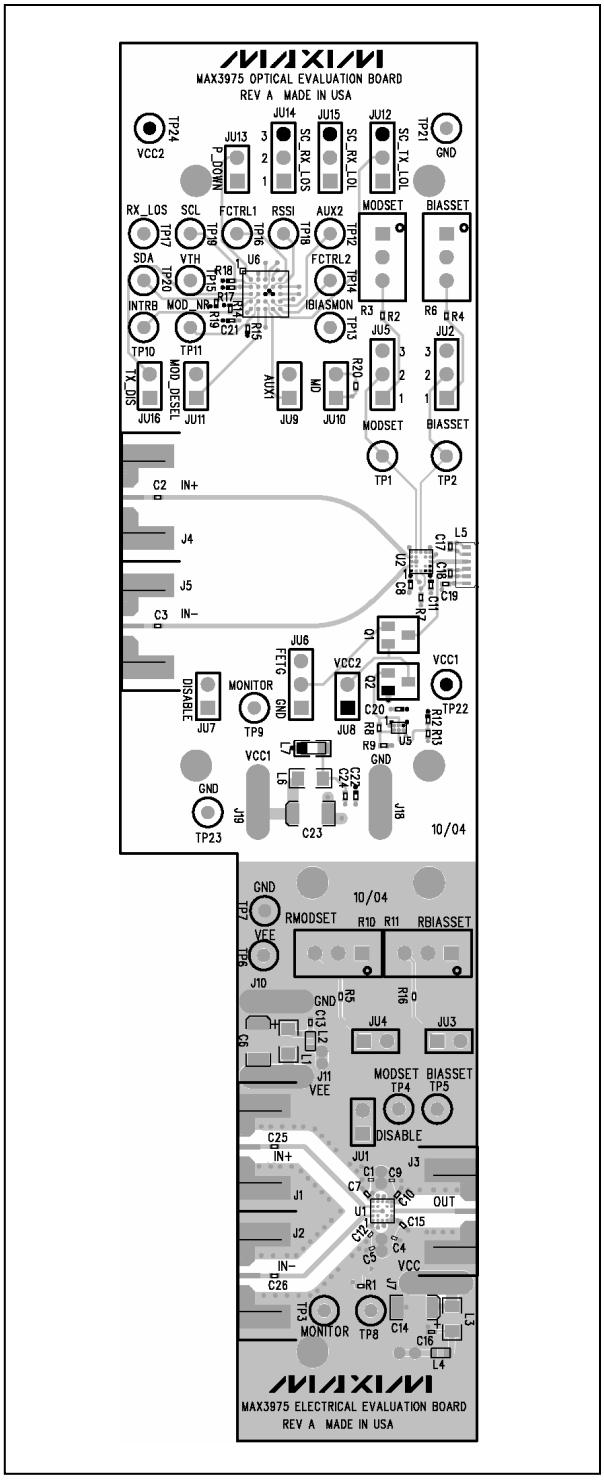

Figure 3. MAX3975 EV Kit Component Placement Guide—Component Side

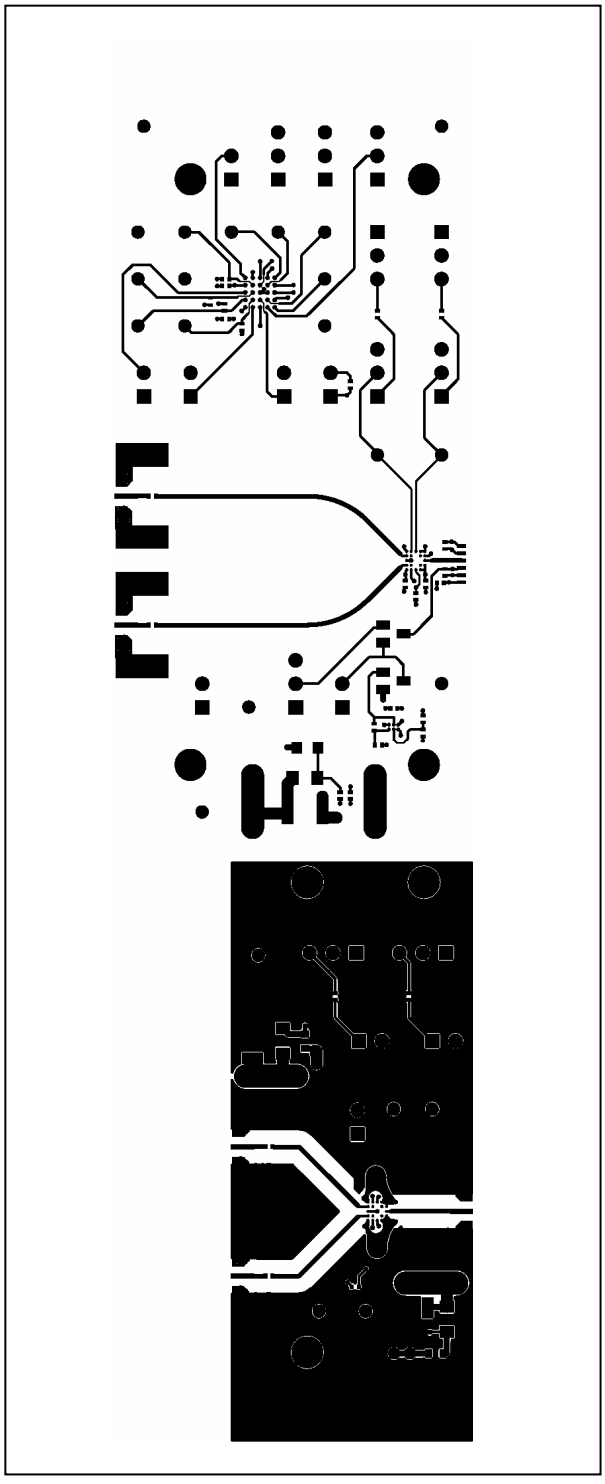

Figure 4. MAX3975 EV Kit PC Board Layout—Component Side

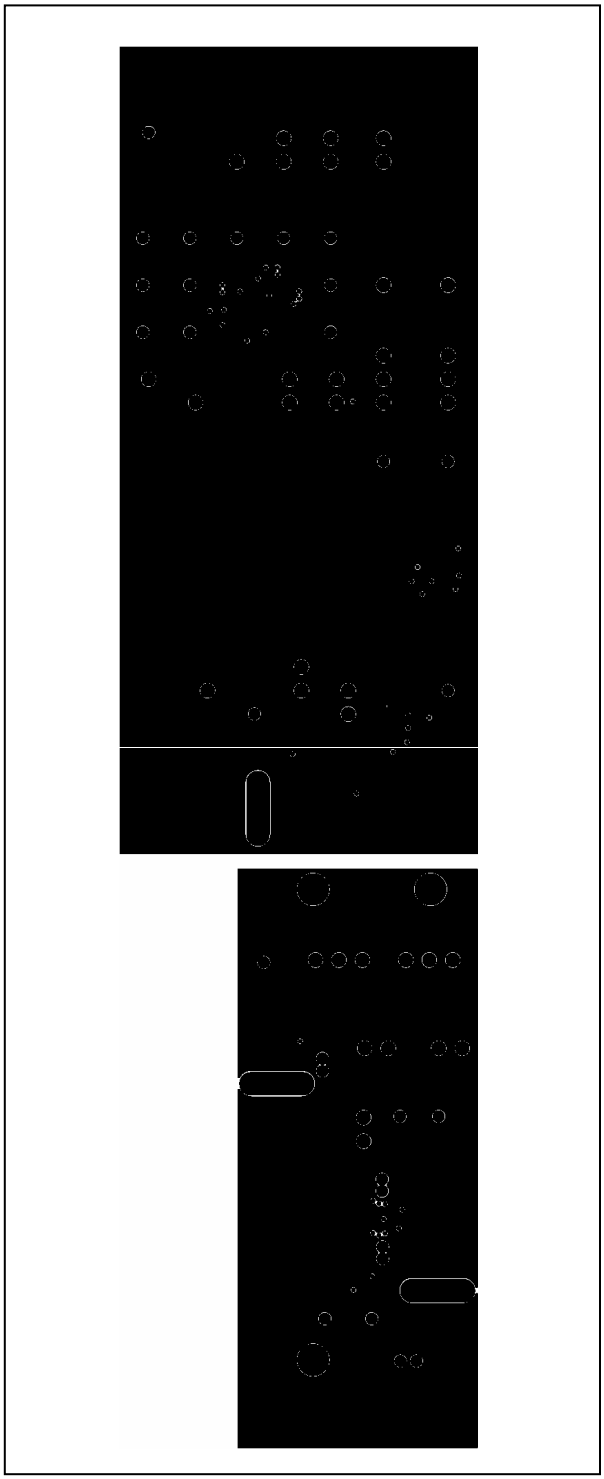

Figure 5. MAX3975 EV Kit PC Board Layout—Ground Plane

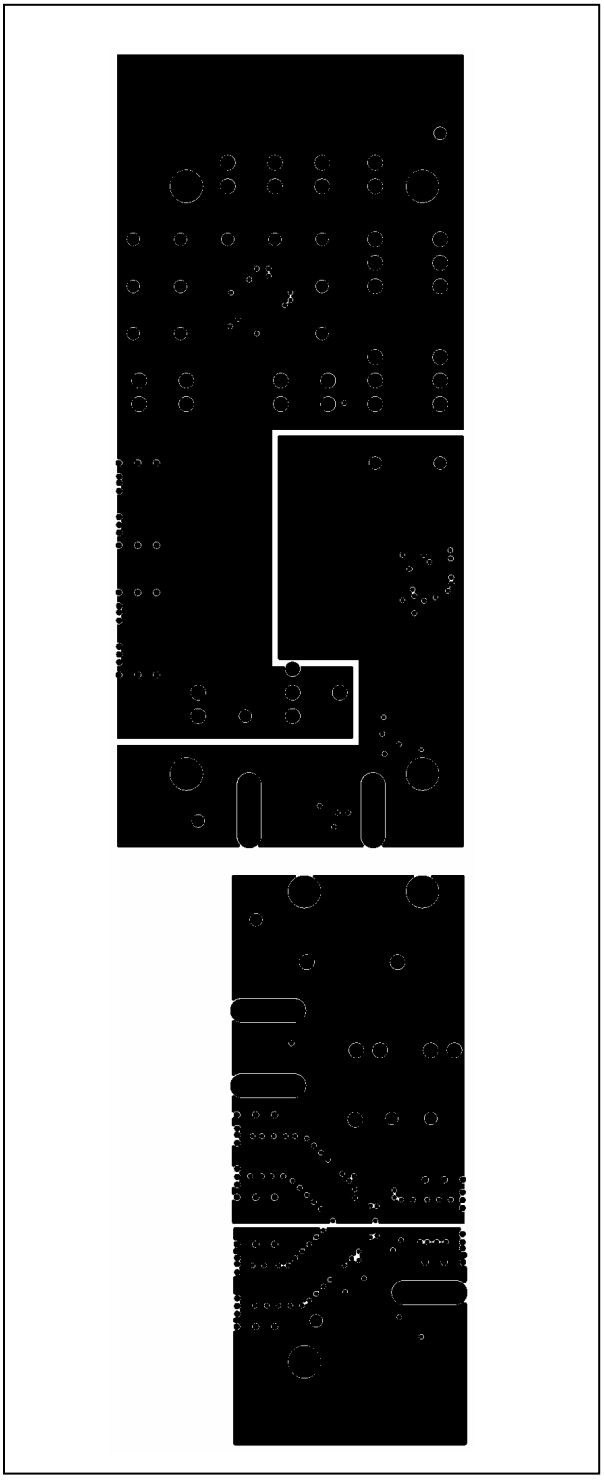

Figure 6. MAX3975 EV Kit PC Board Layout—Power Plane

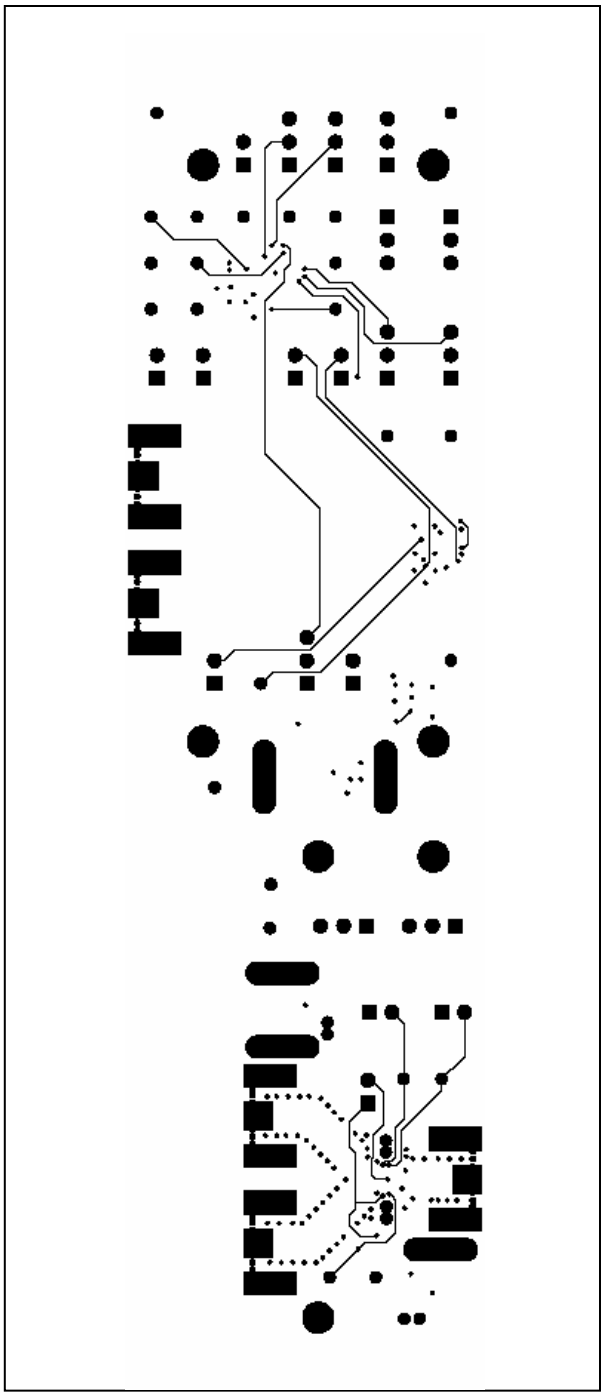

Figure 7. MAX3975 EV Kit PC Board Layout—Solder Side